

U.S. Application Serial No. 09/800,851
Declaration dated January 13, 2005
Filed with Reply to Office Action of October 14, 2004



Attorney Docket No.: 10006513-1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: John F. Hutton et al.

Examiner: Albert C. WANG

Serial No.: 09/800,851

Art Unit: 2115

Filed: March 7, 2001

For: A SCAN BASED MULTIPLE RING OSCILLATOR STRUCTURE FOR
ON-CHIP SPEED MEASUREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

DECLARATION OF JOHN F. HUTTON PURSUANT TO 37 C.F.R. § 1.131

Dear Sir:

1. Prior to June 29, 2000, the filing date of US Patent No. 6,553,545 to Stinson et al., I jointly conceived of at least a method for detecting process variations comprising controlling count gate control by a first circuit, generating at least one clock count by a second circuit, and outputting results of the clock count by a third circuit, as claimed in claims 1-9 of the present application.

2. Prior to June 29, 2000, I jointly conceived of at least an apparatus to detect process variations comprising a first circuit to select a clock, a second circuit connected to the first circuit to generate at least one clock count, and a third circuit connected to the first circuit to output a result of the clock count, as claimed in claims 10-20 of the present application.

3. Prior to June 29, 2000, I jointly conceived of at least a method for detecting process variations comprising controlling count gate control by a first circuit to select a first oscillator, generating a clock by the first oscillator in a second circuit, counting the clock generated by the first oscillator by a third circuit, outputting a count of the clock generated by the first oscillator by the third circuit, selecting a second oscillator in the second circuit, generating a

U.S. Application Serial No. 09/800,851
Declaration dated January 13, 2005
Filed with Reply to Office Action of October 14, 2004

clock by the second oscillator in the second circuit, counting the clock generated by the second oscillator by the third circuit, and outputting a count of the clock generated by the second oscillator by the third circuit, as claimed in claims 21-22 of the present invention.

4. Prior to June 29, 2000, I jointly conceived of at least an apparatus to detect process variations comprising a first circuit to control count gate control, a first oscillator to generate a clock, wherein the first circuit is to select the clock generated by the first oscillator, a second circuit to count the clock generated by the first oscillator and to output the count of the clock generated by the first oscillator, and a second oscillator to generate a clock, wherein the first circuit is to select the clock generated by the second oscillator, and the second circuit is to count the clock generated by the second oscillator and is to output the count of the clock generated by the second oscillator, as claimed in claims 23-24 and 26-29 of the present invention.

5. The attached lab notes dated November 29, 1999, December 15, 1999, and January 26, 2000 show conception of the claimed invention prior to June 29, 2000. *See Exhibit A.*

6. The attached presentation slides dated January 12, 2000 show conception of the claimed invention prior to June 29, 2000. *See Exhibit B.*

7. From February 2000 to July 2000, I, along with my co-inventors, actually reduced the claimed invention to practice including constructing the circuit schematics, creating the circuit artwork, conducting circuit simulations, and testing the final circuit.

8. From immediately prior to June 29, 2000 until the March 7, 2001, the effective filing date of the present application, the claimed invention was constructively reduced to practice with due diligence.

9. On August 15, 2000, I jointly submitted an Invention Disclosure form to Hewlett-Packard's internal Legal Department (HP Legal). *See Exhibit C.* The Invention Disclosure form that I submitted included the brief description, completed on or around August 1, 2000, and diagrams associated with the invention. Such Invention Disclosure forms are submitted so that HP Legal can determine whether to file a patent application.

U.S. Application Serial No. 09/800,851

Declaration dated January 13, 2005

Filed with Reply to Office Action of October 14, 2004

10. On December 28, 2000, I sent draft figures related to the claimed invention to Ami Shah, previously of Dorsey & Whitney LLP.

11. On or about February 4, 2001, I received a draft application describing the claimed invention from Ami Shah.

12. On or about February 6, 2001, I subsequently reviewed the draft application and provided comments to Ami Shah.

13. On or about February 8, 2001, I received a revised draft application describing the claimed invention from Ami Shah.

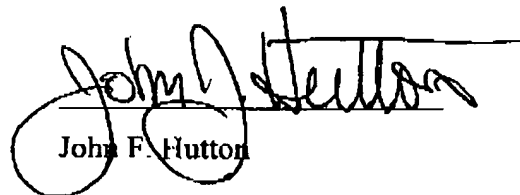
14. On or about February 21, 2001, I subsequently reviewed the revised draft application and provided comments and other feedback.

15. On March 7, 2001, the present application was filed.

16. The acts related above all took place in the United States of America.

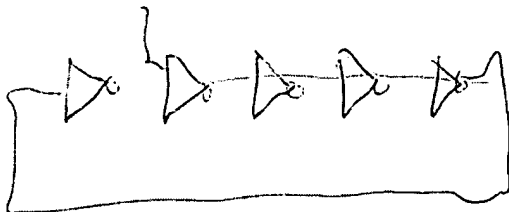
17. The declarant further states that the above statements were made with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of this application or any patent resulting therefrom.

Date: January 13, 2005



John F. Hutton

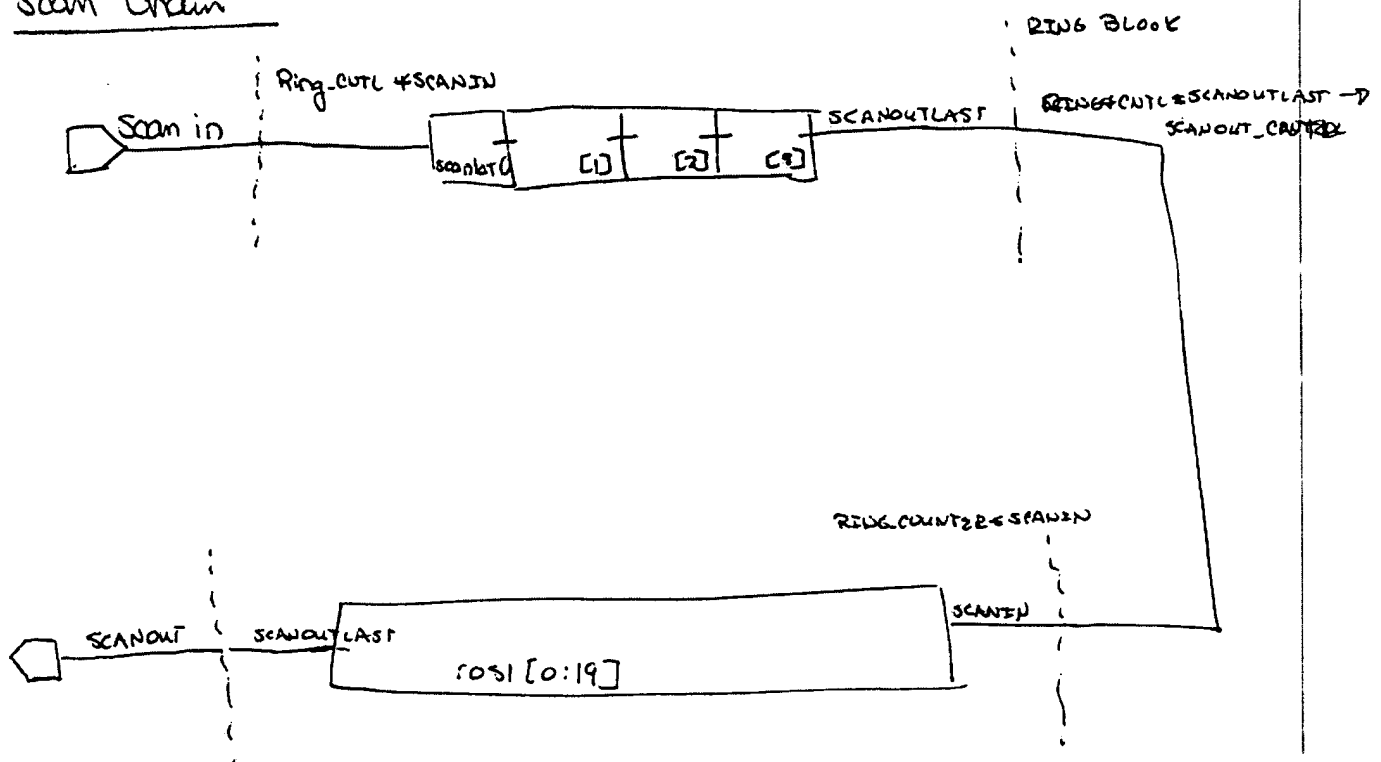
1/27/90
Jh



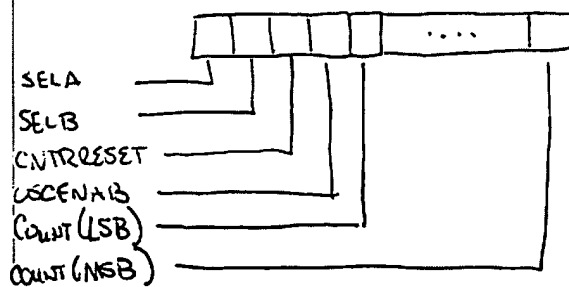
U.S. National Brand

Xcheck Ring

Scan Chain



CNTL[0],[1],[2],[3].ROSL[0],[1],...[19]

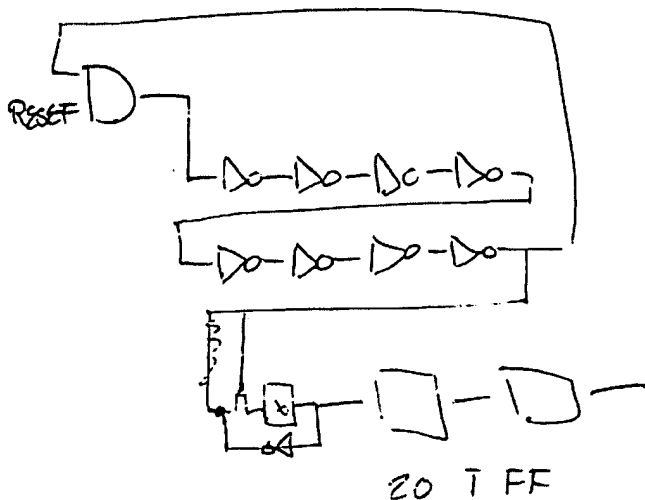


Count will be read in MSB first
 Count will need to be twizzled for proper analysis
 OR - rosl labeling in sch artwork could be changed.

gn
 1/26/06

RING OSCILLATOR

Ripple Counter



for NM case

atches are initialized to one's (FFFFF) so the first count goes to (00000).

The feedback falling to bit 20 falling is

$$1.732 \text{ ns}$$

for the Slow simulation (Some derivation)

$$b9 - b20 \text{ falling} = 2.611 \text{ ns}$$

$$2.611 * \left(\frac{20}{17}\right) = 3.07 \text{ ns}$$

Ring Oscillator StrongN StrongP

LTRAN

$$\text{Nom a StrongN} = 1.236 \text{ ns} (809 \text{ MHz})$$

$$\text{StrongP} = 1.129 \text{ ns} (886 \text{ MHz})$$

NOM

RTRAN

gh
12/15

Ring Oscillator

	<u>Strong N</u>	<u>Balanced</u>	<u>Strong P</u>
LTRAN	1.236 NS	1.236 NS	1.129 NS
NM	1.224 NS	1.224 NS	1.122 NS
RTRAN	1.213 NS	1.213 NS	1.116 NS

With make-cap and l Spice -m nom

LTRAN	1.292	1.292	1.174
NM	1.279	1.279	1.167
RTRAN	1.288	1.268	1.160

I'm seeing no serious effect. It looks like NM is speed gated by the PFET. The big pfet (gated by n fet) is 10% faster in general.

Other ideas -

Drop Cap?

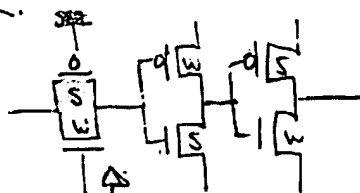
Re balance inverter?

Add some pass fet structures?

Move all the cap to ground or vop on gate?

DAN

For RTRAN LTRAN THE FOLLOWING STRUCTURE MIGHT WORK.



John 12/15

John 12/15

RING OSCILLATOR DESIGN REVIEW

Wednesday, January 12, 2000
10:00 – 11:00 am
6UT12

Tentative Agenda

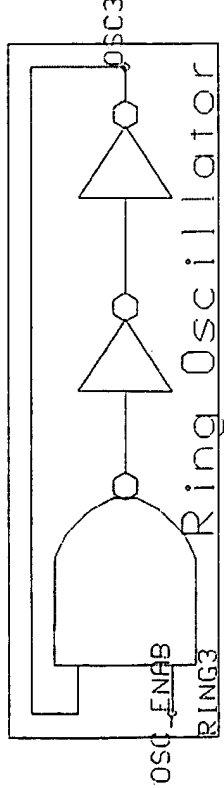
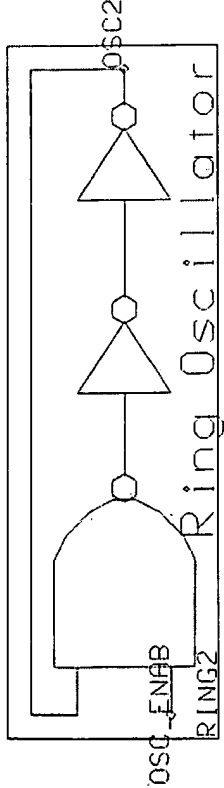
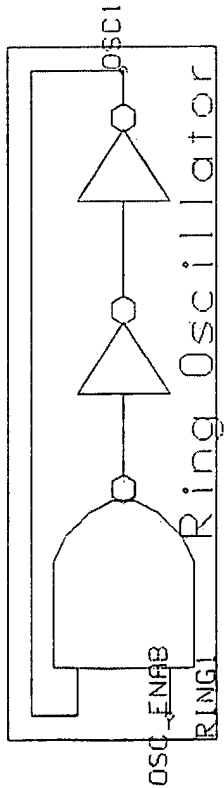
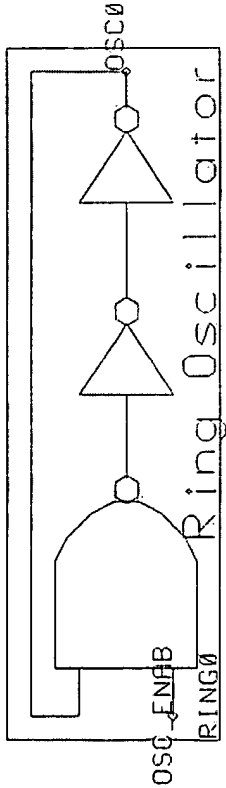
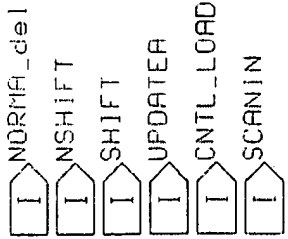
- ▶ Initial Idea (Dan Halperin)
- ▶ Possible Uses
 - Wafer Burn-in Current Detection (Dan H.?)
 - IBM Process Speed Benchmark for Tracking Process Changes (Rick?)
 - Wafer Speed Binning
 - Cross Chip Process Variation (Dan K.)
- ▶ Presentation of Schematics
- ▶ Roundtable

POSSIBLE ROUNDTABLE TOPICS

- ▶ How many ring_block's on the chip? (2, 5, 100s)
- ▶ Is the plan to replace bypass caps in the global route the best way to add these to the chip?
- ▶ How would we gather information for reasonable cross-die process variation?
- ▶ Reset problems? (ENAB should be '0' and OSC_ENAB should be '0')



ring_block1



Generated by bdl2symarc
on 01/10/00 01:23:20 PM MST

SCAN Inputs
OSC/CNF Inputs
Outputs

ring_cntl1

!RING_CNTL*SCANIN=SCANIN
!RING_CNTL*SCANOUTLAST=SCANOUTA

Generated by bdl2symarc
on 01/10/00 01:42:53 PM MST

Scan Ports
Block Ports

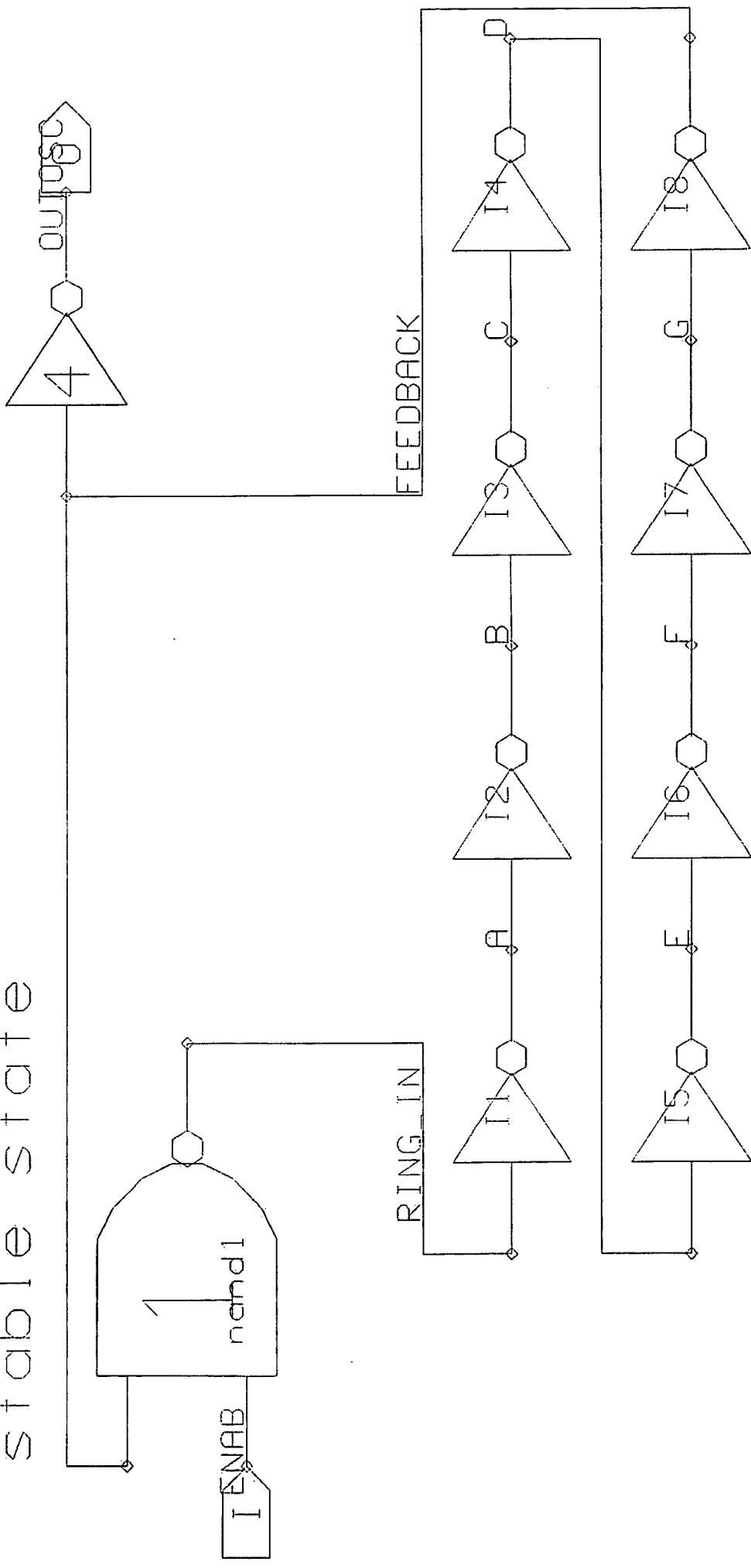
ring_counter

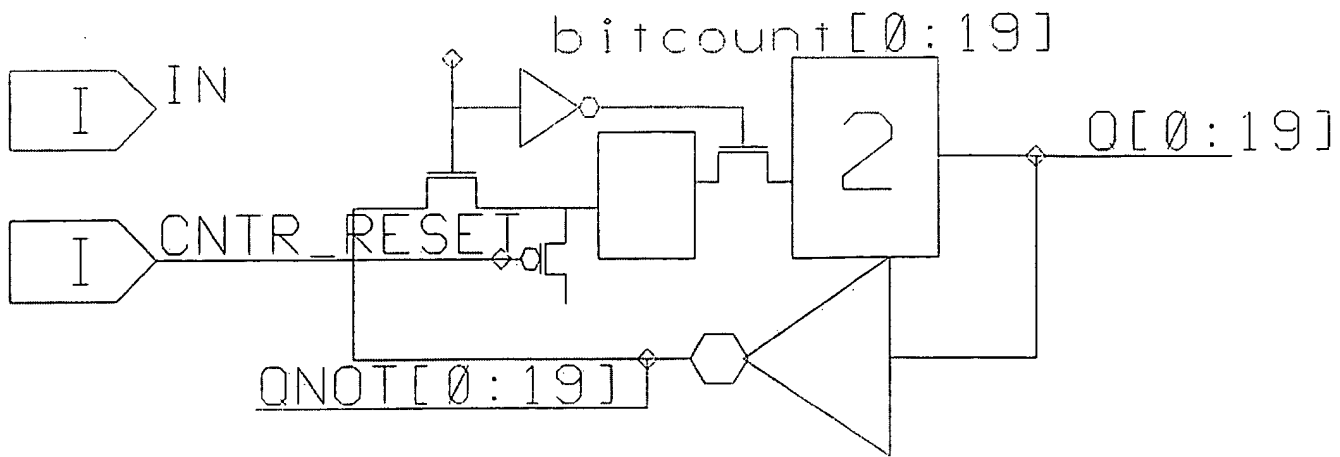
!RING_COUNTER*SCANIN=SCANOUTA
!RING_COUNTER*SCANOUTLAST=SCANOUT

ring-osc

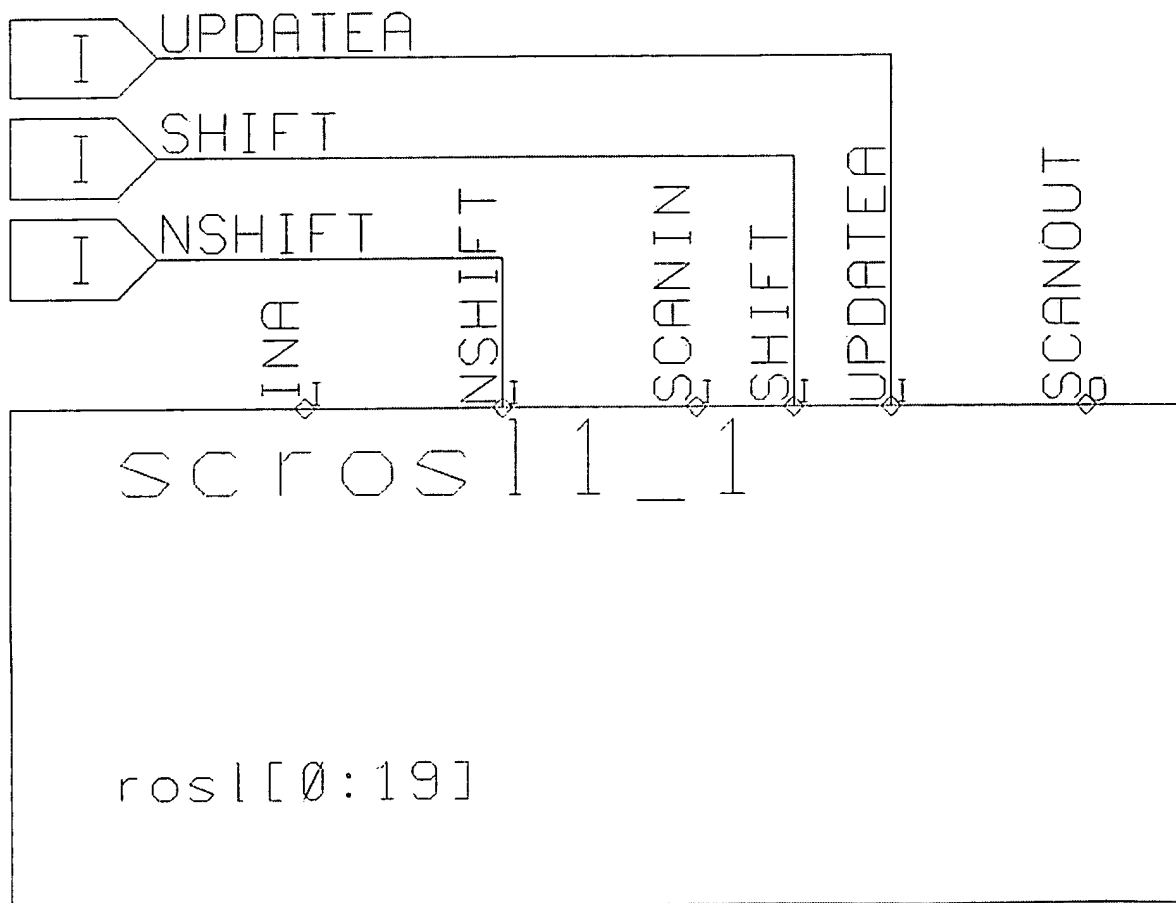
VDD GND

When ENAB is held low the ring will reset to a stable state





!bitcount*T=IN,Q[0:17],QNOT18



!ros]*INA=Q[0:19]
 !ros]*SCANIN=SCANIN,SCANOUT[0:18]
 !ros]*SCANOUT=SCANOUT[0:18],SCANOUTLAST

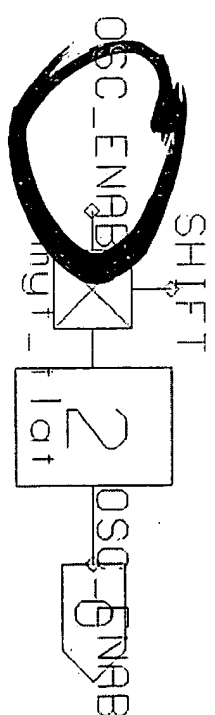
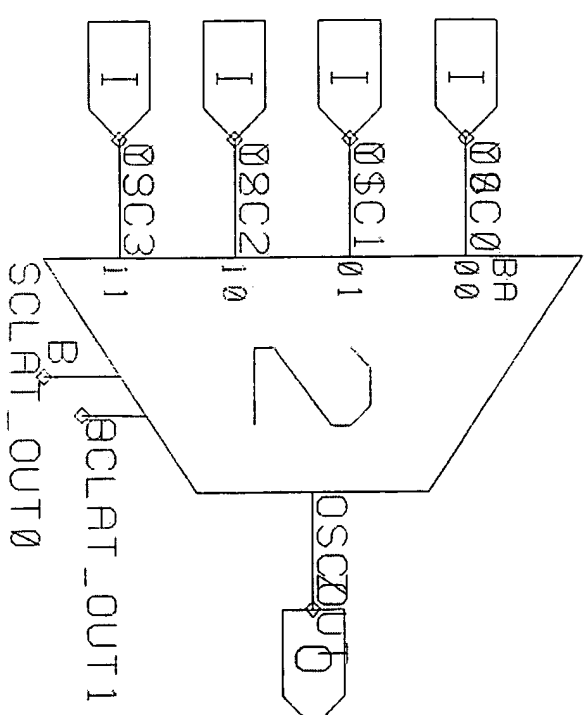
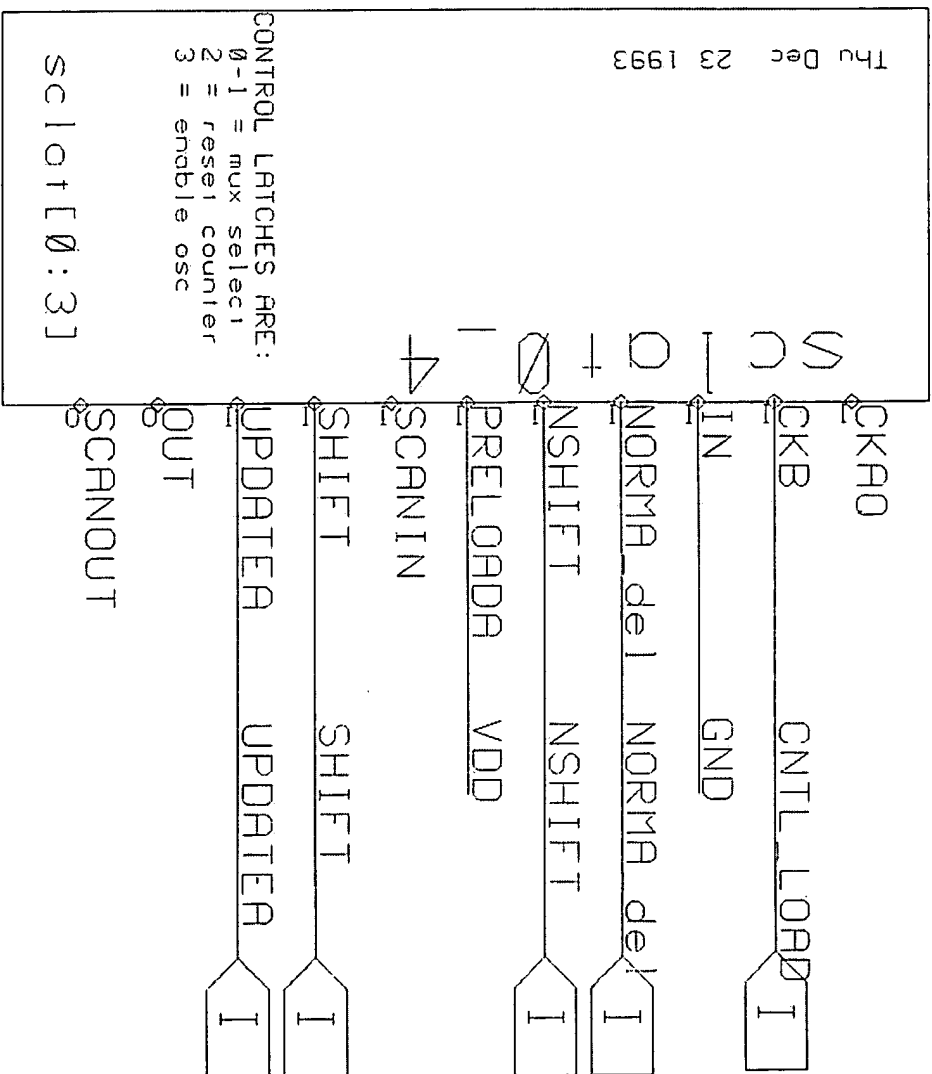
ring_counter1

VDD GND

ring-ctrl1

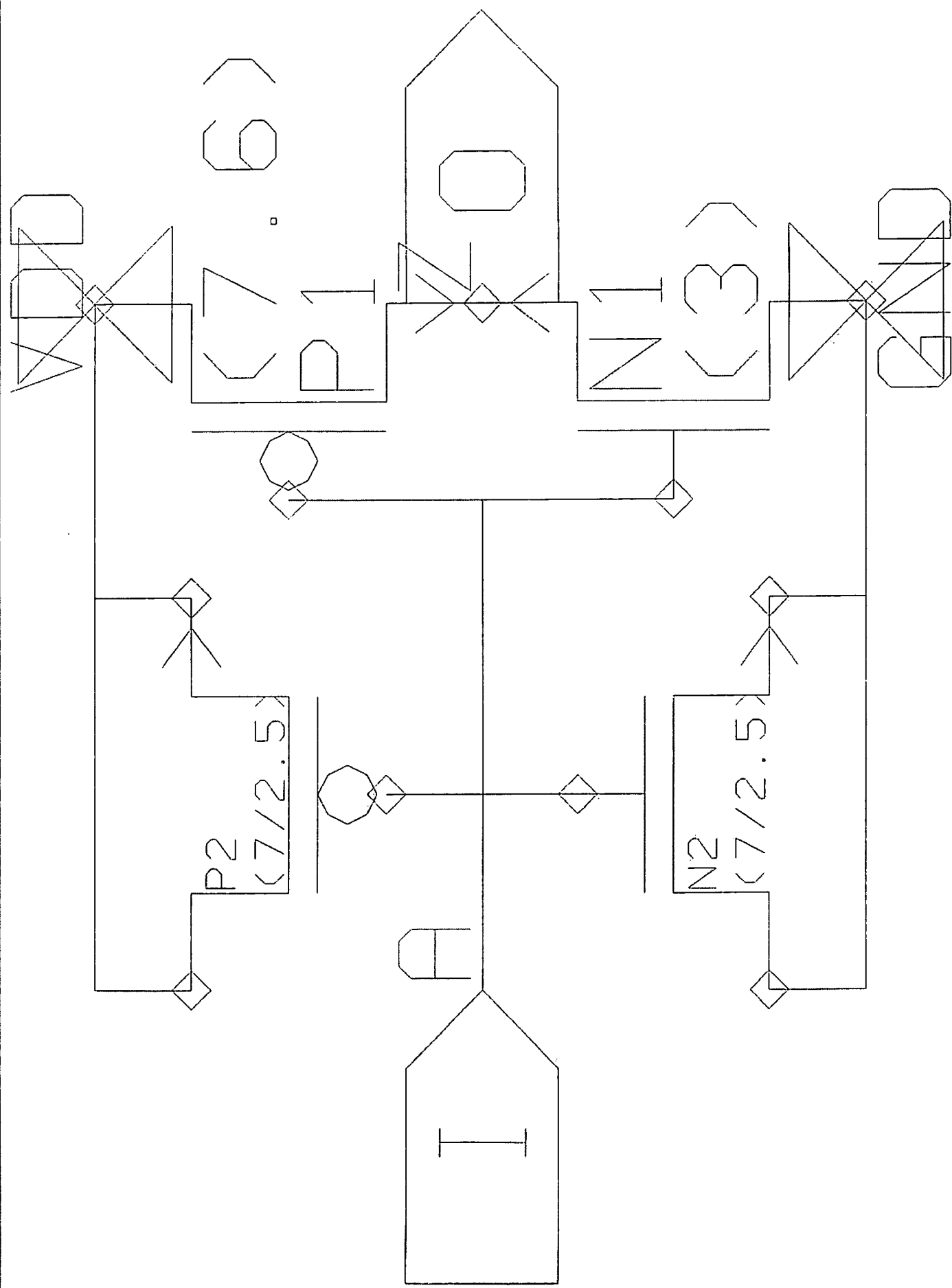
SCANIN I

SCANOUTLASTb

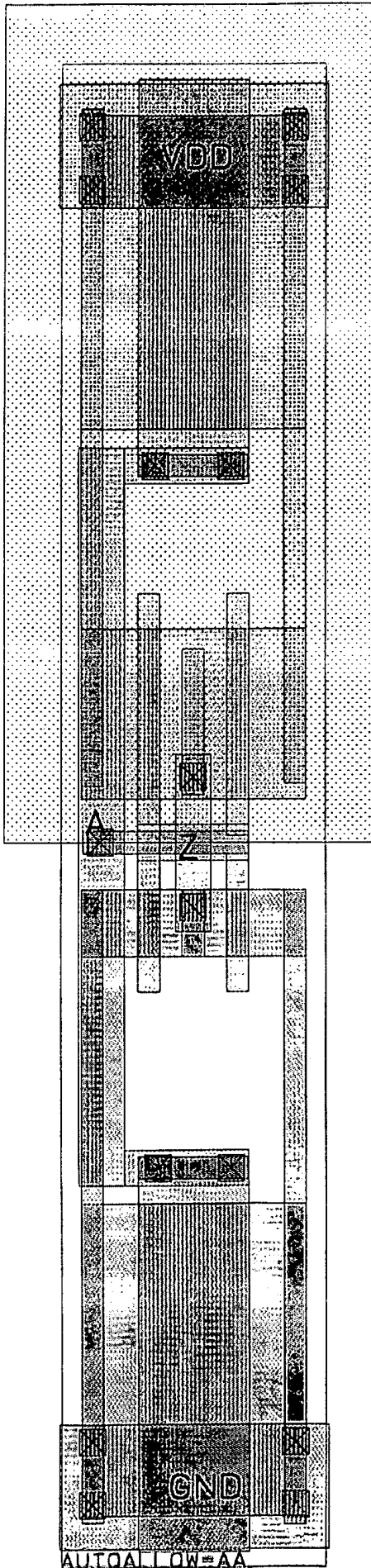


sc | at *CKAO=GND, GND, GND, SHIFT
 sc | at *SCANIN=SCANIN, SCANOUT[0:2]
 sc | at *OUT=SCLAT_OUT0, SCLAT_OUT1, CNTR_RESET, OSC_ENAB
 sc | at *SCANOUT=SCANOUT[0:2], SCANOUTLAST

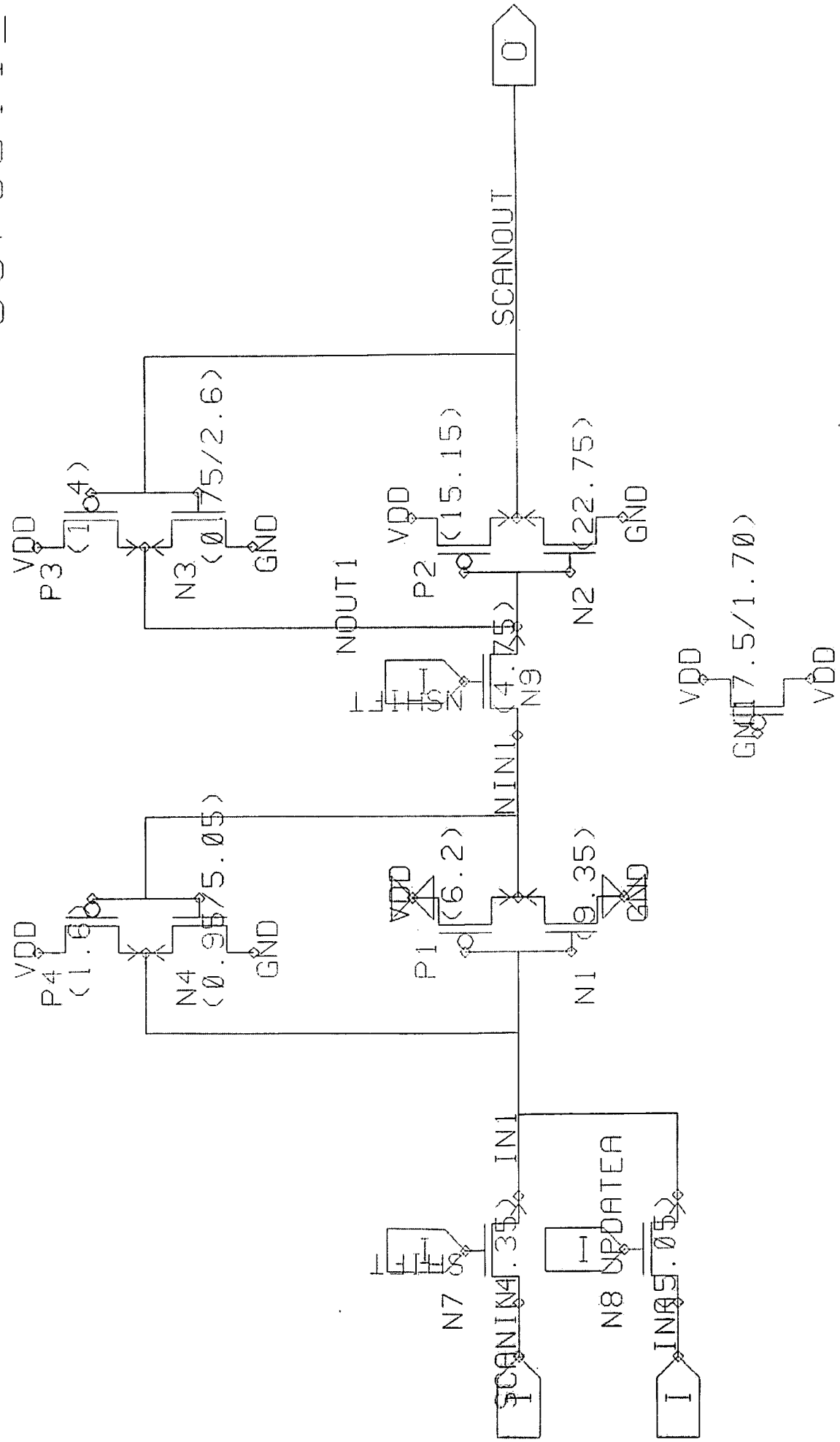
CNTR_RESET
 The reset signal for the counter

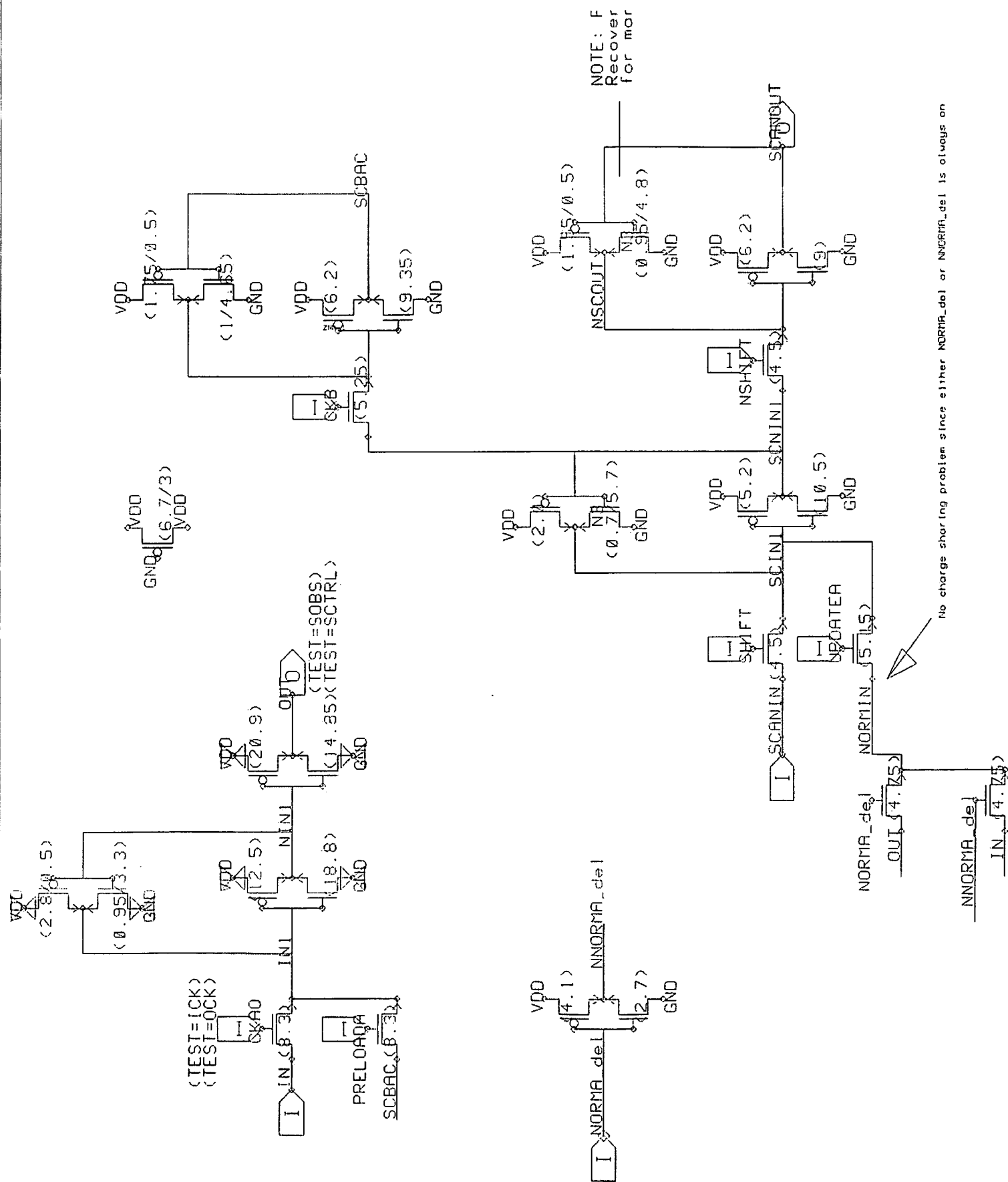


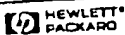
ring_in_v2



SCROS11_1







INVENTION DISCLOSURE

PDNO 10006513

DATE RCVD 8/15/00

PAGE ONE OF

ATTORNEY AJN VTC

Instructions: The information contained in this document is COMPANY CONFIDENTIAL and may not be disclosed to others without prior authorization. Submit this disclosure to the HP Legal Department as soon as possible. No patent protection is possible until a patent application is authorized, prepared, and submitted to the Government.

Descriptive Title of Invention:

Scan based multiple ring oscillator structure for on-chip speed measurement and correlation

Name of Project: Piranha (PCXX? 8600?)

Product Name or Number:

Was a description of the invention published, or are you planning to publish? If so, the date(s) and publication(s):

NO

Was a product including the invention announced, offered for sale, sold, or is such activity proposed? If so, the date(s) and location(s):

NO

Was the invention disclosed to anyone outside of HP, or will such disclosure occur? If so, the date(s) and name(s):

NO

If any of the above situations will occur within 3 months, call your IP attorney or the Legal Department: new at: 1-252-4513 or 570-652-4919

Was the invention described in a lab book or other record? If so, please identify (lab book #, etc.):

Yes - John Hutton's lab book

Was the invention built or tested? If so, the date:

Yes - on current release of Piranha

Was this invention made under a government contract? If so, the agency and contract number:

NO

Description of Invention: Please preserve all records of the invention and attach additional pages for the following. Each additional page should be signed and dated by the inventor(s) and witness(es).

A. Prior solutions and their disadvantages (if available, attach copies of product literature, technical articles, patents, etc.).

SEE ATTACHMENT 1

B. Problems solved by the invention.

Attachment

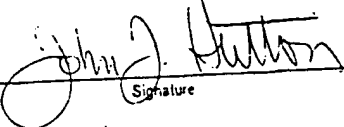
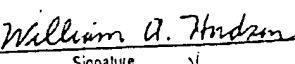
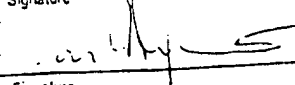
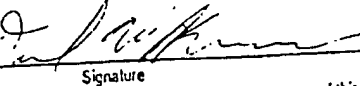
C. Advantages of the invention over what has been done before.

Attachment

D. Description of the construction and operation of the invention (include appropriate schematic, block, & timing diagrams; drawings; samples; graphs; flowcharts; computer listings; test results; etc.)

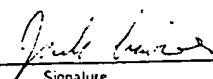
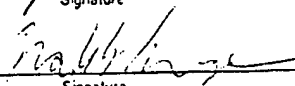
Attachment

Signature of Inventor(s): Pursuant to my (our) employment agreement, I (we) submit this disclosure on:

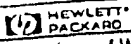
243148	John F. Hutton		898-4497	88	VTC
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
315507	William A. Hudson		898-3458	88	VTC
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
315502	Daniel L. Halperin		898-3273	88	VTC
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
311897	Daniel W. Krueger		898-2236	88	VTC
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name

(If more than four inventors, include additional information on another copy of this form and attach to this document)

Signature of Inventor(s): Pursuant to my (our) employment agreement, I (we) submit this disclosure on:

244155	Jack T. Lavier		898-0404	88	VTC
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
243034	Mark D. Musgrove		898-7895	88	VTC
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name

(If more than four inventors, include additional information on another copy of this form and attach to this document)

	INVENTION DISCLOSURE	COMPANY CONFIDENTIAL	PAGE <u> </u> OF <u> </u>
Signature of Witness(es): (Please try to obtain the signature of the person(s) to whom invention was first disclosed.)			
The invention was first explained to, and understood by, me (us) on this date: <u> </u>		Date of Signature <u> </u>	
Full Name <u> </u>		Signature <u> </u>	
Full Name <u> </u>		Date of Signature <u> </u>	

Inventor & Home Address Information: (If more than four inventors, include addl. information on a copy of this form & attach to this document.)

Inventor's Full Name			
John F. Hutton			
Street		State	Zip
1562 Faraday Circle		CO	80525
City		State	Zip
Fort Collins			
Do you have a Residential P.O. Address? P.O. BOX <u> </u>			
Greeted as (nickname, middle name, etc.)		Citizenship	
John		USA	

Inventor's Full Name			
William A. Hudson			
Street		State	Zip
5204 Greenview Drive		CO	80525
City		State	Zip
Fort Collins			
Do you have a Residential P.O. Address? P.O. BOX <u> </u>			
Greeted as (nickname, middle name, etc.)		Citizenship	
Bill		USA	

Inventor's Full Name			
Daniel L. Halperin			
Street		State	Zip
4336 Arcada Court		CO	80525
City		State	Zip
Fort Collins			
Do you have a Residential P.O. Address? P.O. BOX <u> </u>			
Greeted as (nickname, middle name, etc.)		Citizenship	
Dan		USA	

Inventor's Full Name			
Daniel W. Krueger			
Street		State	Zip
1437 Sanford Drive		CO	80526
City		State	Zip
Fort Collins			
Do you have a Residential P.O. Address? P.O. BOX <u> </u>			
Greeted as (nickname, middle name, etc.)		Citizenship	
Dan		USA	



INVENTION DISCLOSURE

COMPANY CONFIDENTIAL

PAGE ____ OF ____

Signature of Witness(es): (Please try to obtain the signature of the person(s) to whom invention was first disclosed.)

The invention was first explained to, and understood by, me (us) on this date: _____

Date of Signature

Full Name

Signature

Date of Signature

Full Name

Signature

Date of Signature

Inventor & Home Address Information: (If more than four inventors, include add'l information on a copy of this form & attach to this document.)

Inventor's Full Name
Jack T. LavierStreet
1640 Kirkwood Drive, Apt. 2136

1514

Imperial

State

Zip

City
Fort Collins

CO

80525

Do you have a Residential P.O. Address? P.O. BOX

City

State

Zip

Greeted as (nickname, middle name, etc.)
JackCitizenship
USAInventor's Full Name
Mark D. MusgroveStreet
5907 Auburn Drive

State

Zip

City
Fort Collins

CO

80525

Do you have a Residential P.O. Address? P.O. BOX

City

State

Zip

Greeted as (nickname, middle name, etc.)
MarkCitizenship
USA

Inventor's Full Name

Street

State

Zip

City

State

Zip

Do you have a Residential P.O. Address? P.O. BOX

City

State

Zip

Greeted as (nickname, middle name, etc.)

Citizenship

Inventor's Full Name

Street

State

Zip

City

State

Zip

Do you have a Residential P.O. Address? P.O. BOX

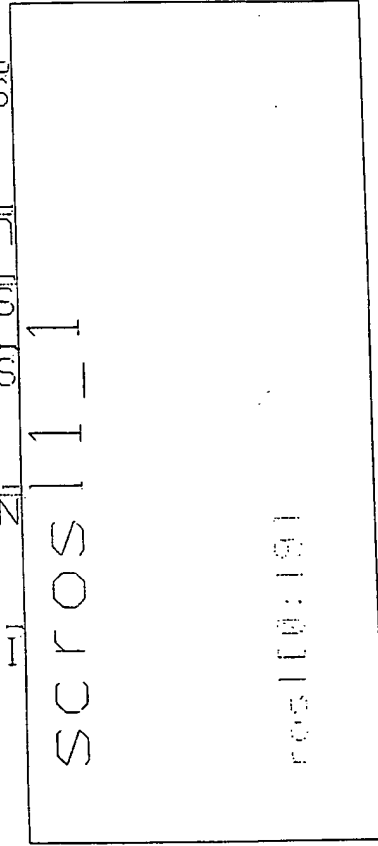
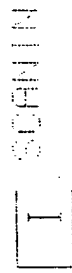
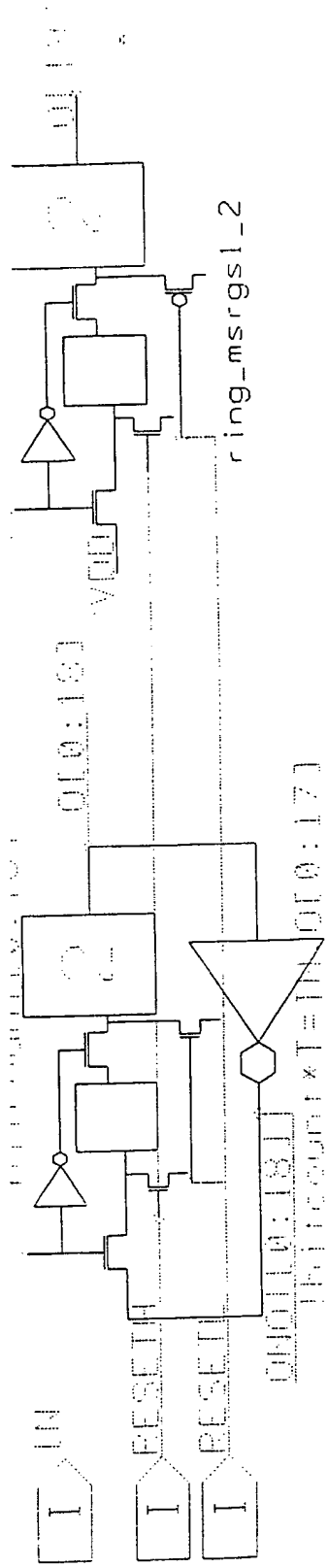
City

State

Zip

Greeted as (nicknames, middle name, etc.)

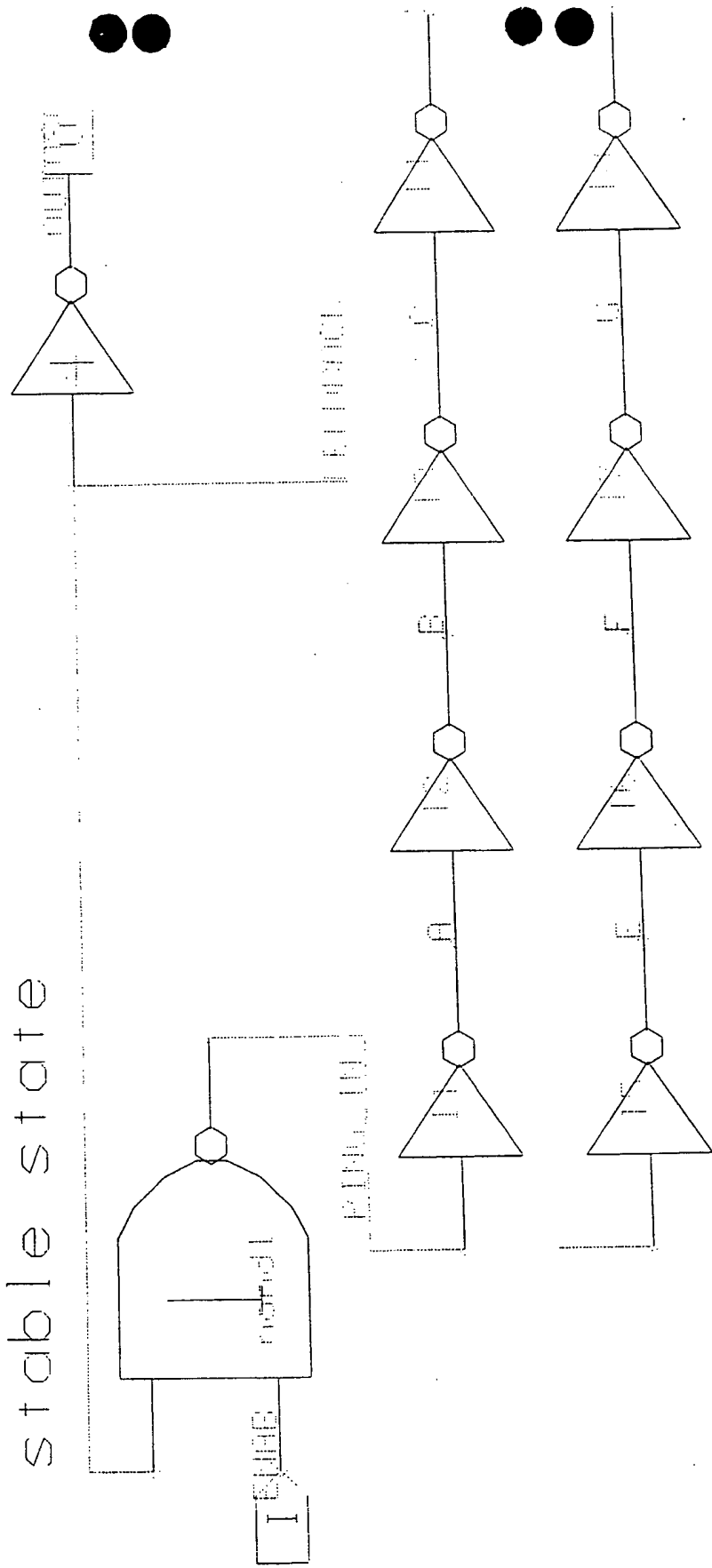
Citizenship

[illegible]

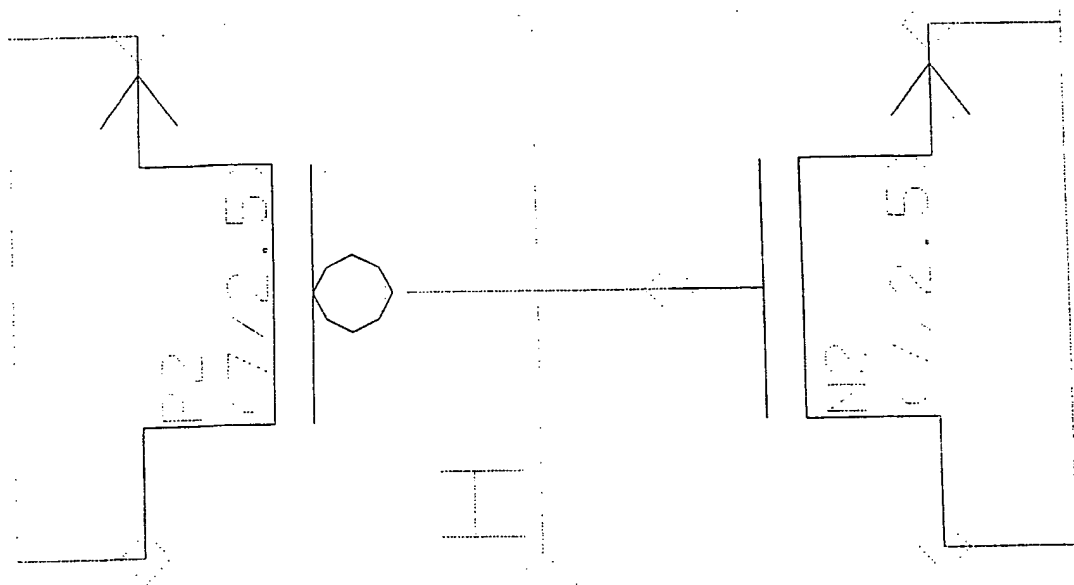
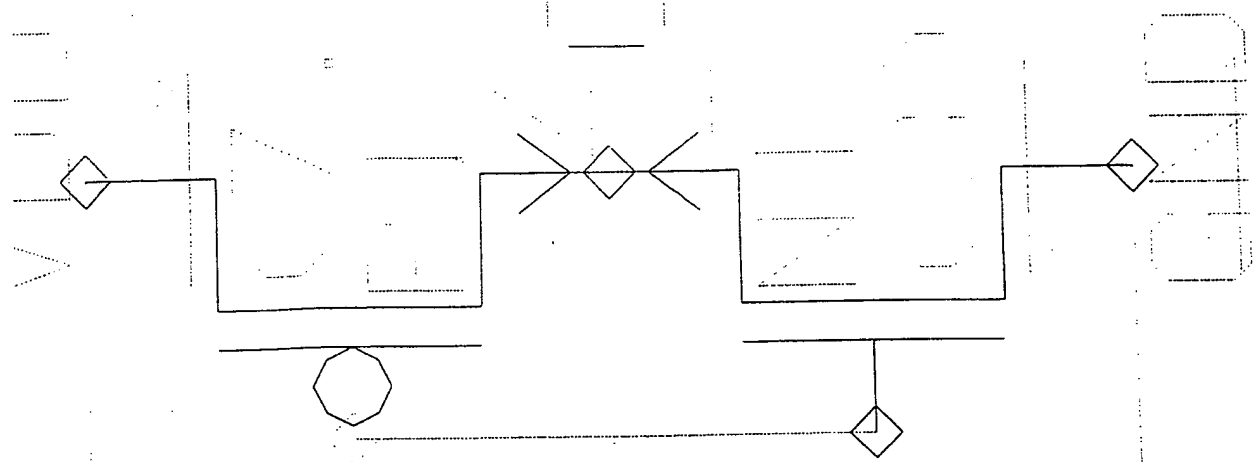
ring_counter1

100-443887-10

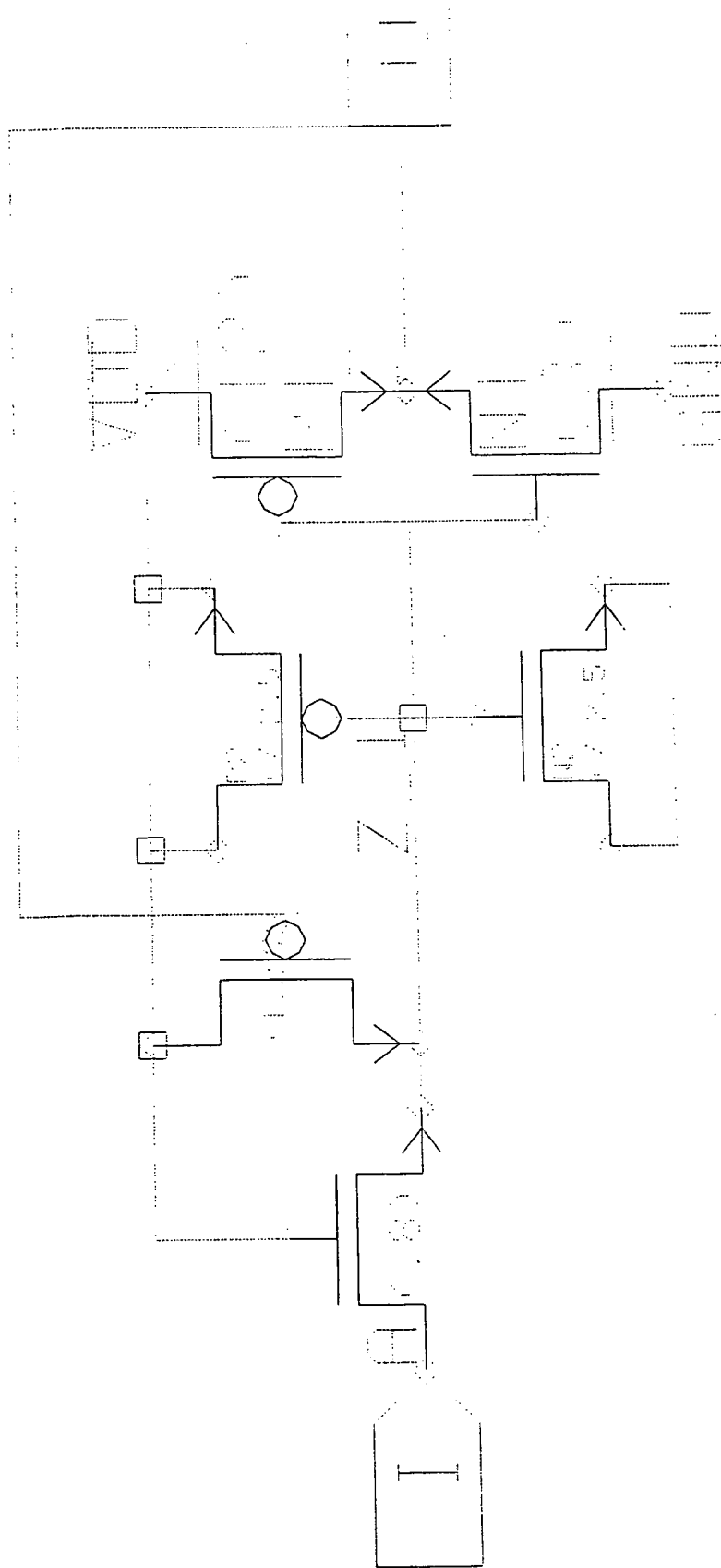
When ENAB is held low
the ring will reset to a
stable state



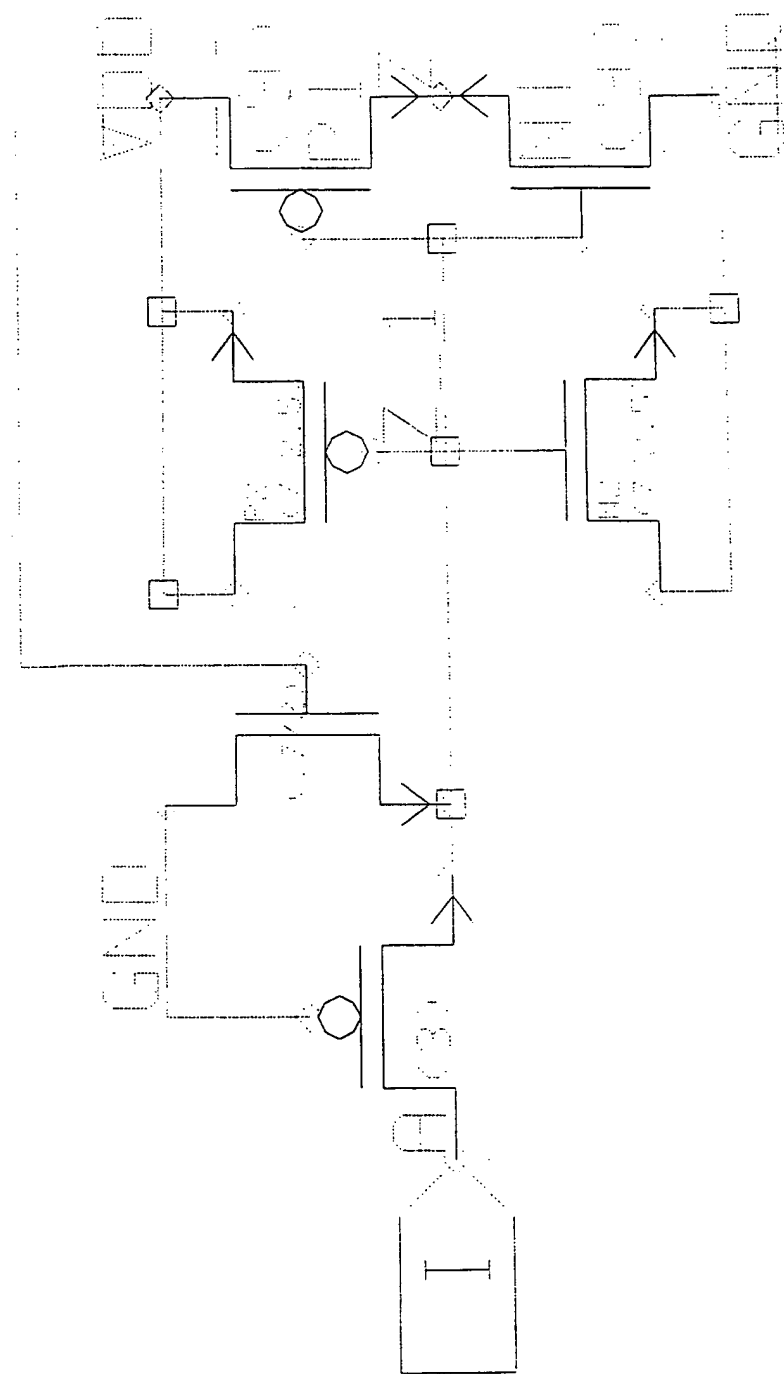
100-1



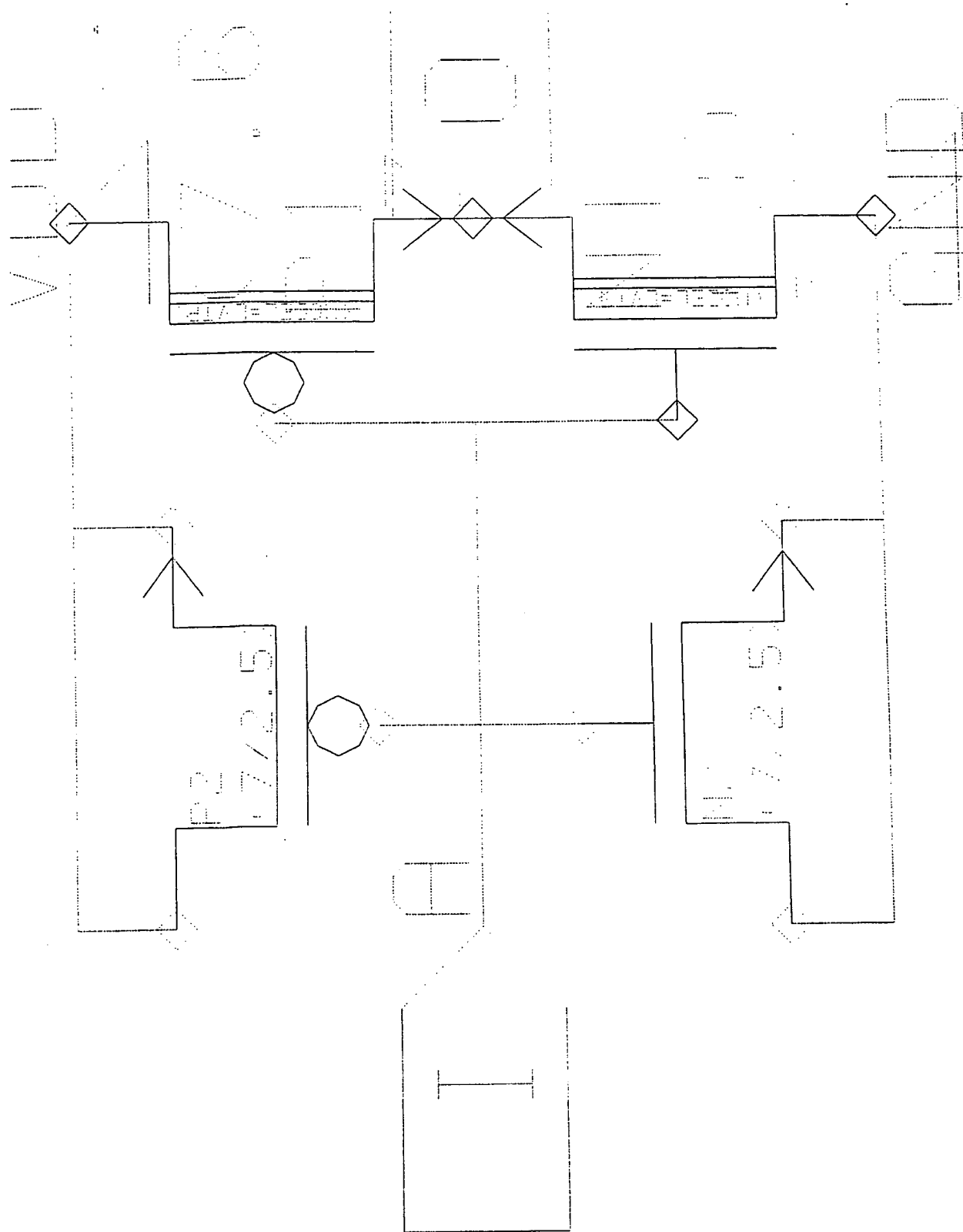
ring-invl



ring_inv2



ring_invrtran1



1 + > | > U i o | O C i L

Alex -- Here is the bulk of my invention disclosure form with the schematic attachments. The form is attached as well as a slew of schematics from this block. Please let me know if you would like any more information.

Sincerely,

John Hutton

FNL -- 3UPJ, 0x84497, john_hutton@hp.com, jfh@fc.hp.com

-----X-----X-----X-----X-----X-----X-----X-----X-----X-----X-----

Ring Oscillator Invention Disclosure Form

Description of Invention

A. Prior solutions and their disadvantages

Speed binning is usually done based upon some type of broadside test done by a package tester. For piranha, the fuses that normally hold this information on the die are laser blowable, not electrically blowable. This means that some method to get a "best guess" at the speed of the part at wafer test will significantly reduce the price of packaging a part that will not make the frequency cutoff.

Some type of ring oscillators are often used in the analog parameter testing (APT) structures generated by the wafer manufacturer. However these tests are run by the fab which saves the information in a database. This does not help set the speed bin of the part at wafer test.

While I have heard of other ring oscillator structures (sadly no references) placed on a chip to attempt to compensate for process variation, I believe their affect was always to local circuits. They did not export their information outside of the chip.

B. Problems solved by this invention

This simple device bundles 4 ring oscillators, a 20-bit ripple counter, and the necessary control logic to a JTAG scan based interface. It is on every die, so that each location can be individually tested (APT sites tend to be scattered throughout the wafer). It communicates with the outside world through the standard JTAG interface. It is accessible at wafer, package, and system test which allows for several methods of correlating the oscillator speed to the speed of a part in an actual system. It is much simpler than a broadside test, and should directly track significant process variations.

C. Advantages

Simple. Tracks process. On every die. Accessible at wafer for early speed binning. Accessible through the wafer, package, and system test lifecycle which allows for accurate oscillator to system speed correlation.

D. Description of the construction and operation

This structure has three main parts: the oscillators, the counter, and the control. All of the relevant schematic and artwork plots will be attached to the end of this write-up.

The oscillators were build from simple fet structures. Each fet has a 'fet capacitor' type load to allow a reasonable frequency with a low number of stages. This also simulated a rise time on the order of 150 ps, which would be reasonable for a clock on this processor. The four oscillators are:

Normal oscillator, 8 stages, 800 MHz nominal frequency

LTran oscillator, added an N-fet pass transistor, 200 MHz nominal
RTran oscillator, added an P-fet pass transistor, 200 MHz nominal
Low Vt oscillator, the normal with Low Vt fets.

The L- and R-tran structure, at least in spice, had stronger dependences on the handedness of the process. We hope that this would allow us to keep better track of major process variations.

The counter was a simple 20-bit ripple counter with an asynchronous reset. It was composed of T-flip flops. While the ripple time was on the order of milliseconds, the scan control had no way of operating that fast. The danger of having an error related to ripple is almost non-existent.

The control is the heart of the structure. Since this circuit is entirely scan driven, we have to be able to reset, select one of the four oscillators, control the start and stop of the count, latch and scan out the final count. The 'start and stop' is the most critical segment of this block.

Two control bits select the oscillator. One control bit triggers a reset of the counter. The final bit is the enable line.

In order to accurately control the time that the counter is on, we set up a simple state machine that looks for two successive SHIFT-rising on the scan clock. This is a signal that the tester can control with a very high precision. The input scan vector disables the reset, selects the oscillator, and enables the count. On the next SHIFT clock, the counter is gated on. On the subsequent SHIFT clock, the counter is gated off. Then the count can be transferred back to the scan chain and shifted out.

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.